

a semiconductor substrate in which a desired circuit element is being formed, the surface of said insulating film being partially exposed[, the top level metal being separated by intra-layer dielectric];

[Depositing] depositing a passivation layer over said top-level metal and over the partially exposed surface of said insulating layer, [intra-level dielectric] said passivation layer comprising a first and a second passivation layer;

AS  
cont.-  
[Depositing] depositing a layer of photosensitive polyimide over said passivation layer;

[Patterning] patterning and etching said layer of photosensitive polyimide thereby forming a pattern for said bonding pads;

[Patterning] patterning and etching said passivation layer thereby exposing said bond pad, said patterning and etching of said passivation layer to take place after said patterning and etching of said layer of photosensitive polyimide; and

[Curing] curing and cross-linking said photosensitive polyimide said curing and cross-linking of said photosensitive polyimide to take place after said patterning and etching of said passivation layer.

2. (Amended) The method of claim 1 wherein said [top level metal contains] top level interconnecting metal for interconnecting lines and said top level bond pad metal for bond pads comprises Aluminum.

AS  
end

3. (Amended) The method of claim 1 wherein said [top level metal contains] top level interconnecting metal for interconnecting lines and said top level bond pad metal for bond pads comprises aluminum/copper (Al/Cu) alloy.

5. (Amended) The method of claim 1 wherein said [passivation layer is a] first passivation layer [of] comprises Plasma Enhanced oxide deposited to a thickness of about 2000 Angstrom, [over which a] said second passivation layer [of] comprises Plasma Enhanced  $\text{Si}_3\text{N}_4$  [is] deposited to a thickness of about 7000 Angstrom.

A/b

8. (Amended) The method of claim 1 wherein the thickness of said photosensitive polyimide is within the range of between 5.0 and 9.5  $\mu\text{m}$  [ $\mu\text{m}$  Angstrom] after deposition of said photosensitive polyimide whereby shrinkage of up to 40% of said thickness could occur after curing of said layer of photosensitive polyimide.

A7  
Sub D<sup>2</sup>

15. (Amended) The method of claim 1 wherein said [top level

AS  
C<sub>1</sub>

C

TSMC98-403

Serial number 09/285,986

Sub  
C1  
end

interconnecting metal and top-level bond pad metal] top level metal for interconnecting lines and top level metal for bond pads are formed within or on top of any layer of a semiconductor device other than or in addition to said semiconductor substrate.

A8  
end

16. (Amended) The method of claim 1 wherein said [top level interconnecting metal and top-level bond pad metal] top level metal for interconnecting lines and top level metal for bond pads are formed selectively on the bare main surface of a semiconductor substrate in which a desired circuit element is being formed.

Sub D6

20. (Amended) A method of forming planarized bonding pads within the structure of a semiconductor device comprising the steps of:

A9

providing a semiconductor substrate, said semiconductor substrate to contain electrical circuits or other electrical functional electrical components;

providing a wiring layer having wiring and having a plurality of bond pads having a thickness, the wiring of said wiring layer being directly connected to said bond pads in addition to being connected to said electrical circuits or other electrical functional components within said semiconductor

TSMC98-403

Serial number 09/285,986

substrate, the wiring layer being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the surface of said insulating layer being partially exposed [, said wiring and said bond pads being separated by intra-layer dielectric];

depositing a layer of top metal over said [bonding] bond pads thereby depositing [the bonding] bond pad metal;

AG  
Cont.  
depositing a passivation layer over said [top level metal interconnecting lines] wiring layer and over said [top level metal] bond [pads] pad metal and over the exposed surface of the [intra-level dielectric] insulating layer [thereby shielding said bond pads from damage during subsequent packaging operations];

depositing a layer of photosensitive polyimide over said passivation layer to a thickness within the range of between 5.0 and 9.5 μm [um Angstrom];

patterning and etching said layer of photosensitive polyimide thereby forming a pattern of photosensitive polyimide said pattern being identical to the pattern of said bond pads, partially removing said photosensitive polyimide from above the surface of said bond pads;

etching said layer of [photosensitive polyimide] passivation, thereby removing said [photosensitive polyimide]

TSMC98-403

Serial number 09/285,986

passivation above said [planarized] bond pads, said patterning and etching of said passivation layer to take place after said patterning and etching said layer of photosensitive polyimide;  
and

curing and cross-linking said photosensitive polyimide thereby protecting the underlying circuitry said curing and cross-linking of said photosensitive polyimide to take place after said etching of said passivation layer.

21. (Amended) The method of claim 20 wherein said [top level metal] wiring and said plurality of bond pads comprise [contains] aluminum.

22. (Amended) The method of claim 20 wherein said [top level metal] wiring and said plurality of bond pads comprise [contains] aluminum/copper (Al/Cu) alloy.

23. (Amended) The method of claim 20 wherein the thickness of said [bonding pad] bond pads is the thickness of said top level metal, said thickness being within the range of between 4000 and 8000 Angstroms.

A10  
25. (Amended) The method of claim 20 wherein said patterning said layer of photosensitive polyimide is creating a pattern that is above [and mates with] said plurality of bond pads.

✓  
26. Please cancel claim 26.

A11  
27. (Amended) The method of claim 20 wherein that portion of said photosensitive polyimide that remains after completion of said patterning and etching said photosensitive polyimide [is not removed but] is left in place to serve as a stress buffer and to [thereby] provide protection against damage and extrusion of that portion of the surface of the passivation layer which is not removed by etching.

IN THE DRAWINGS

The text has been amended to include a reference #10 that is indicated in Figs. 8 and 9.